IFW

500.43057X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: H. MATSUSHIGE, et al

Serial No.: 10/649,687

Filed: August 28, 2003

For: STORAGE UNIT AND CIRCUIT FOR SHAPING COMMUNICATION SIGNAL

PETITION TO MAKE SPECIAL
UNDER 37 CFR 1.102(d) and MPEP. §708.02, VIII

MS Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

July 22, 2004

Sir:

1. Petition

Applicants hereby petition to make this application **Special**, in accordance with 37 CFR §1.102(d) and MPEP 708.02, VIII. The present invention is a new application filed in the United States Patent and Trademark Office on August 28, 2003 and as such has not received any examination by the Examiner.

2. Claims

Applicants hereby represent that all the claims in the present application are directed to a single invention. If upon examination it is determined that all the claims presented are not directed to a single invention, Applicants will make an election without traverse as a prerequisite to the granting of special status.

07/23/2004 EABUBAK1 00000074 10649687
01 FC:1460 130.00 OP

3. Search

Applicants hereby submit that a pre-examination search, a copy of which is attached, has been made by a professional searcher in the following classes and subclasses:

Class	Subclasses	Description
318/		ELECTRICITY: MOTIVE POWER SYSTEMS
	603	Pulse-counting systems
324/		ELECTRICITY: MEASURING AND TESTING
	207.25	Rotary
360/		**DYNAMIC MAGNETIC INFORMATION STORAGE OR RETRIEVAL**
	51	. Data clocking
	69	AUTOMATIC CONTROL OF A RECORDER MECHANISM
	73.02	... Control of relative speed between carriers
	73.03	... Rotary carrier
710/		**ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT**
	15	. Peripheral monitoring
	58	. Input/Output process timing
711/		**ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY**
	101	. Specific memory composition
	112	... Direct access storage device (DASD)
	117	. Hierarchical memories
	147	. Shared memory area
	167	. Access timing
	170	. Memory configuring

The above subclasses represent areas deemed to contain subject matter of interest to one or more of the search features. Please note that relevant references may be classified outside of these areas. The integrity of the search is based on the records as presented by the United States Patent and Trademark Office (USPTO). No further integrity studies were performed. Also a key word search was performed on the USPTO full-text database including published U.S. patent applications.

4. Copy of References

A listing of all references found by the professional searcher is provided by a Form PTO-1449 and copies of the references and the Form PTO-1449 are submitted as part of an Information Disclosure Statement (IDS) filed on even date.

5. Detailed Discussion of the References and Distinctions Between the References and the Claims

Below is a discussion of the references uncovered by the search and cited in the IDS filed on even date that appear to be most closely related to the subject matter encompassed by the claims of the present application, and which discussion particularly points out how Applicants' claimed subject matter is distinguishable over those references. All other references uncovered by the search and cited in the IDS filed on even date are **not** treated in detail herein.

a. Detailed Discussion of the References

Aikawa et al. (U.S. Patent No. 5,155,638), assigned to Teac Corporation, provides for a *Compatible Data Storage Apparatus for Use with Disk Assemblies of Two or More Different Storage Capacities*. Discussed is a compatible data storage

apparatus having a transducer for writing and reading data on first and second replaceable disk assemblies of different storage capacities at first and second data transfer rates under control of a host system. Two disk sensors may be employed for discriminating between two different types of disks, preferably there may also be included a mode means for inputting from the host system a mode signal indicative of first a first mode in which data is written and read at first and second data transfer rate (see column 1, lines 58-63 and column 2, lines 18-21and 24-28).

Olarig et al. (U.S. Patent No. 6,530,007 B2), assigned to Compaq Information Technologies Group, L.P., provides a *Method and Apparatus for Supporting Heterogeneous Memory in Computer Systems.* Discussed is a memory controller capable of supporting heterogeneous memory configurations. The memory controller receives a memory request, identifies a memory and also memory access parameters, and accesses the memory and returns or stores the request. A RAM personality module or memory controller in a second tier is clocked by the same clock received by the first memory controller in the memory system controller (see column 2, lines 41-44 and 47-50, and column 3, lines 2-5).

Piccirillo et al. (U.S. Patent Application Publication No. 2002/0053010 A1) provides for a *Method for Supporting Multi-Level Stripping of Non-Homogeneous Memory to Maximize Concurrency.* Discussed are host/data controllers **16/18** to be further coupled to one or more memory controllers. Each of the memory controllers **20A-20E** is further coupled to a segment of main memory (see paragraph 42).

Nagase et al. (U.S. Patent Application Publication No. 2003/0140207 A1), assigned to Hitachi, Ltd., provides a *Hierarchical Storage Apparatus and Control Apparatus Thereof.* Disclosed is a storage apparatus including a hierarchical storage

unit with a first storage device having a first access speed and a second storage device having a second access speed. Storage controller **201** handles read and write requests to the various storage devices **301**, **302**, **303** and **304** provided in the hierarchical storage area **300**. The controller **201** receives write and read requests from one or more hosts and temporarily stores a corresponding data block in a cache memory **203** (see figure 4, and paragraphs 11 and 33).

b. Distinctions Between the References and the Claims

The present invention as recited in the claims is not taught or suggested by any of the above noted references whether taken individually or in combination with each other or in combination with any of the other references now of record.

The present invention as now recited in the claims is directed to a storage unit which includes a channel control portion for receiving a data input/output request, a cache memory for storing data, a disk control portion for performing input/output processing on data in accordance with the data input/output request, and a plurality of disk drives for storing data. At least two of the disk drives input data to and output data from the disk control portion at different communication speeds. Further, according to the present invention, the storage unit has a plurality of communication paths provided to connect at least one of the disk drives in such a manner as to constitute a loop defined by the FC-AL fiber channel standards, so that the communication speeds can be set differently for these different communication paths.

The above described features of the present invention, particularly the provision wherein at least two of the disk drives of the storage unit input data to and

output data from a disk control portion of the storage unit at different communication speeds and the provision that the storage unit has a plurality of communication paths provided to connect at least one of the disk drives in such a manner as to constitute a loop defined by the FC-AL fiber channel standards, so that the communication speeds can be set differently for these different communication paths are taught or suggested by any of the references of record whether taken individually or in combination with each other.

6. Fee (37 C.F.R. 1.17(i))

The fee required by 37 C.F.R. § 1.17(i) is to be paid by:

[X] the Credit Card Payment Form (attached) for $130.00.

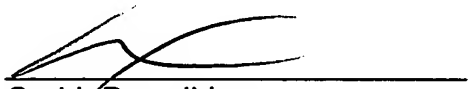
[ ] charging Account _____ the sum of $130.00.

A duplicate of this petition is attached.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (500.43057X00).

Respectfully submitted,

Antonelli, Terry, Stout & Kraus, LLP



Carl I. Brundidge
Registration No. 29,621

CIB/jdc
Enclosures

500.43057X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: H. MATSUSHIGE, et al

Serial No.: 10/649,687

Filed: August 28, 2003

For: STORAGE UNIT AND CIRCUIT FOR SHAPING COMMUNICATION SIGNAL

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §1.97 & 1.98

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

July 22, 2004

Sir:

In the matter of the above-identified application, applicants are submitting herewith copies of the documents listed in the attached form equivalent to Form PTO-1449 for the Examiner's consideration.

This information disclosure statement is being submitted before the mailing date of a first office action on the merits.

Each of the documents listed on the attached form equivalent to Form PTO-1449 is in the English language.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus Deposit Account No. 01-2135 (500.43057X00) please credit any excess fees to such deposit account.

Respectfully submitted,

Carl I. Brundidge
Registration No. 29,621
ANTONELLI, TERRY, STOUT & KRAUS, LLP

CIB/jdc
(703) 312-6600

FORM PTO-1449 U.S. Department of Commerce (Rev. 4/92) Patent and Trademark Office

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
500.43057X00	10/649,687
APPLICANT: H. MATSUSHIGE, et al	
FILING DATE: August 28, 2003	GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER							DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		5	1	5	5	6	3	8	10/92	Aikawa et al			
		5	4	3	0	8	5	5	7/95	Walsh et al			
		6	5	3	0	0	0	7	3/03	Olarig et al			
	2002	0	0	0	4	8	9	2	1/02	Gans et al			
	2002	0	0	5	3	0	1	0	5/02	Piccirillo et al			
	2003	0	1	4	0	2	0	7	7/03	Nagase et al			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	ABSTRACT	
							YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation is considered, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

(Form PTO-1449 [6-4])

LACASSE & ASSOCIATES, LLC

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May 28, 2004

津村 W1156-01
10/649687 EH

Via Federal Express
Noboru Otsuka
Hitachi, Ltd.
IP Development & Management Division
Patent Dept. 4
292, Yoshida-cho, Totsuka, Yokohama-shi
Kanagawa, Japan 244-0817

RE: PATENTABILITY SEARCH FOR STORAGE UNIT AND CIRCUIT FOR SHAPING COMMUNICATION SIGNAL
Your File: 340300352US01
Our Docket: PSP-1041430

Dear Ms. Otsuka:

In accordance with your request, we have conducted a patentability search on the above-identified subject matter.

Enclosed with this report are copies of the search results and your disclosure materials. If after reviewing the results, you feel that the search feature (or specific search elements), the field of search, or results are not commensurate with your original request, or you would like to extend the search into additional areas, please contact us.

Sincerely,

R. W. Lacasse

Randy W. Lacasse

Enclosures
RWL:IT:eah
s04/psp1041430

CONFIDENTIAL
(Patentability Search)

I. SEARCH FEATURE

A. General

Storage unit and circuit for shaping communication signal.

B. Specific

A storage unit comprising:

a channel control portion for receiving a data input/output request;

a cache memory for storing data;

a disk control portion for performing input/output processing on data in accordance with said data input/output request; and

a plurality of disk drives for storing data,

wherein at least two of said disk drives input data to and output it from said disk control portion at different communication speeds.

C. Application

II. FIELD OF SEARCH

The search of the above features was conducted in the following areas:

A. Classification search

Class	Subclasses	Description
318/		**ELECTRICITY: MOTIVE POWER SYSTEMS**
	603	.. Pulse-counting systems
324/		**ELECTRICITY: MEASURING AND TESTING**
	207.25	.. Rotary

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	51	. Data clocking
	69	AUTOMATIC CONTROL OF A RECORDER MECHANISM
	73.02	... Control of relative speed between carriers
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710/		**ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT**
	15	. Peripheral monitoring
	58	. Input/Output process timing
711/		**ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY**
	101	. Specific memory composition
	112	... Direct access storage device (DASD)
	117	. Hierarchical memories
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The above subclasses represent areas deemed to contain subject matter of interest to one or more of the search features. Please note that relevant references may be classified outside of these areas. The integrity of the search is based on the records as presented to us by the United States Patent and Trademark Office (USPTO). No further integrity studies were performed. Also a key word search was performed on the USPTO full-text database including published U.S. patent applications.

III. RESULTS OF SEARCH

A. References developed as a result of search (related art is in boldface):

U.S. Patent No.	Inventor
5,155,638	**Aikawa et al.**
5,430,855	Walsh et al.
6,530,007 B2	**Olarig et al.**

U.S. Patent Application Publication No.	Inventor
2002/0004892 A1	Gans et al.

U.S. Patent Application Publication	Inventor (continued)
2002/0053010 A1	**Piccirillo et al.**
2003/0140207 A1	**Nagase et al.**

B. Discussion of related references in numerical order:

The patent to Aikawa et al. (5,155,638), assigned to Teac Corporation, provides for a *Compatible Data Storage Apparatus for Use with Disk Assemblies of Two or More Different Storage Capacities.* Discussed is a compatible data storage apparatus having a transducer for writing and reading data on first and second replaceable disk assemblies of different storage capacities at first and second data transfer rates under control of a host system. Two disk sensors may be employed for discriminating between two different types of disks, preferably there may also be included a mode means for inputting from the host system a mode signal indicative of first a first mode in which data is written and read at first and second data transfer rate (see column 1, lines 58-63 and column 2, lines 18-21and 24-28).

The patent to Olarig et al. (6,530,007 B2), assigned to Compaq Information Technologies Group, L.P., provides for a *Method and Apparatus for Supporting Heterogeneous Memory in Computer Systems.* Discussed is a memory controller capable of supporting heterogeneous memory configurations. The memory controller receives a memory request, identifies a memory and also memory access parameters, and accesses the memory and returns or stores the request. A RAM personality module or memory controller in a second tier is clocked by the same clock received by the first memory controller in the memory system controller (see column 2, lines 41-44 and 47-50, and column 3, lines 2-5).

The patent application publication to Piccirillo et al. (2002/0053010 A1) provides for a *Method for Supporting Multi-Level Stripping of Non-Homogeneous Memory to Maximize Concurrency.* Discussed are host/data controllers **16/18** to be further coupled to one or more memory controllers. Each of the memory controllers **20A-20E** is further coupled to a segment of main memory (see paragraph 42).

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corresponding data block in a cache memory **203** (see figure 4, and paragraphs 11 and 33).

Iuliana Tanase

Iuliana Tanase ~~EAH~~